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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/990,093	11/21/2001	Jeffrey Binder	BCS04507	1287

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EXAMINER	
CHOWDHURY, SUMAIYA A	

ART UNIT	PAPER NUMBER
2623	

NOTIFICATION DATE	DELIVERY MODE
01/30/2008	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

Docketing.Schaumburg@motorola.com
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Office Action Summary	Application No.	Applicant(s)	
	09/990,093	BINDER ET AL.	
	Examiner	Art Unit	
	Sumaiya A. Chowdhury	2623	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08 November 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *28-33* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *28-33* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. Applicant's arguments with respect to claims 28-33 have been considered but are moot in view of the new ground(s) of rejection.

(a) Applicant argues "Thus, Rege describes receiving..." on page 7, 3rd paragraph of the Remarks filed 11/8/07.

In response, the Examiner has brought in Cannella to teach this limitation.

(b) Applicant argues "Rege does not have a dedicated piece of hardware, such as the claimed backplane interface, for inputting data into the disk array..." on page 8, 1st paragraph of the Remarks filed 11/8/07.

The Examiner disagrees with the Applicant. Referring to Fig, 2 in Rege, there are three servers 300 which both receive and transmit data to and from disks 800. The Examiner interprets the first two servers 300 to be the first and second stream server modules, and interprets the third server 300 to be the backplane interface. Referring to col. 3, lines 60-64, Rege teaches multimedia is transferred from server 300 to the disk storage 800. Hence, the claim limitation of a backplane interface which forwards content to a memory is met.

(c) Applicant argues "Control lines 403 ..." on page 8, 2nd paragraph of the Remarks filed 11/8/07.

In response, the Examiner has brought Singh to teach this limitation.

(d) Applicant argues "...replaces the disks of Rege..." on page 8, 3rd paragraph of the Remarks filed 11/8/07.

In response, the Examiner has brought Hooper to teach this limitation.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 28-30, and 33 are rejected under 35 U.S.C. 103(a) as being unpatentable over Rege in view of Rebec (5619528), Cannella (5854840), Singh (5966722) and Hooper (5414455).

As for claim 28, Rege teaches a system for distributing content comprising:

a memory array (redundant array 800) that stores content – col. 5, lines 37-45;

a first stream server module (first server 300) comprising;

a first stream server processor (cpu 310 – fig. 3) that requests content (The processor within server 300 requests content from disk 800 - col. 3, lines 28-33);

a first media access controller (cpu 310) that receives the content (The content is accessed sequentially – col. 6, lines 47-59); and

a first media interface module (321, 331, 341 – fig. 3) which transmits the content from the first media access controller into a format for a physical interface (The data is formatted according to the corresponding interface it is transmitted to. In other words, if it is transmitted to a WAN, it is formatted accordingly. - col. 3, lines 42-56);

a backplane interface (server 300) that forwards content to the disk array (800) (Multimedia is transferred from server 300 to disk array 800);

a second stream server module (second server 300); and

an interconnect (switch 400) connected to the memory, the first stream server module, the second stream server module, and the backplane interface (fig. 2; col. 3, line 64 – col. 4, line 9) comprising;

a data bus (Lines 401, 402, 403) coupled between first stream server module and the memory array and coupled between the second stream server module and the memory array and coupled between the backplane interface and the semiconductor array that carries content (Lines 401, 402, and 403 allow switching elements 500 to connect the servers 300 to the disks 800. The content

along with its corresponding destination address is transmitted over lines 401, 402, and 403 – col. 3, line 64 – col. 4, line 15); and

an arbitrator (600) that determines which of the first stream server module and the second stream server module may access either the address bus or the data bus based and which of the first stream server module and the second stream server module has priority (col. 3, lines 35-41, col. 3, line 64-col. 4, line 8, col. 5, line 10-18).

Wherein the interconnect forwards content from the backplane interface to the semiconductor memory and forwards content from the semiconductor memory to the first stream server module (col. 3, lines 30-63);

However, Rege fails to teach:

Content is forwarded in a time frame relative to the latency of a semiconductor memory;

A server processor that encodes content;

A media access controller that receives encoded content and serializes the received encoded content for physical layer transport;

an address bus larger than 32 bits wide that carries content addresses;

In an analogous art, Rebec teaches a server processor (843F) that encodes content (col. 11, lines 30-37) and a media access controller (851F) that receives the encoded content (col. 11, lines 30-37);

It would have been obvious to one of ordinary skill in the art at the time of applicant's invention to modify Rege's invention to include the above mentioned

limitation, as taught by Rebec, for the well known advantage of converting the data for transmission.

However, Rege and Rebec fails to teach:

Content is forwarded in a time frame relative to the latency of a semiconductor memory;

Serializing received content for physical layer transport;

an address bus larger than 32 bits wide that carries content addresses;

In an analogous art, Cannella teaches serializing data for physical layer transport (col. 4, lines 30-45).

It would have been obvious to one of ordinary skill in the art at the time of applicant's invention to modify Rege and Rebec's invention to include the above mentioned limitation, as taught by Cannella, in order to format the data as needed by the physical layer transport.

However, Rege, Rebec, and Cannella fail to teach:

Content is forwarded in a time frame relative to the latency of a semiconductor memory;

an address bus larger than 32 bits wide that carries content addresses;

In an analogous art, Singh teaches:

an address bus larger than 32 bits wide that carries content addresses (col. 4, line 63 – col. 5, line 8);

It would have been obvious to one of ordinary skill in the art at the time of applicant's invention to modify Rege, Rebec, and Cannella's invention to include

the above mentioned limitation, as taught by Singh, in order to be able to access large memory arrays.

However, Rege, Rebec, and Cannella fail to teach:

Content is forwarded in a time frame relative to the latency of a semiconductor memory;

In an analogous art, Hooper teaches video server 22 includes semiconductor memory for storing video data (col. 4, lines 40-45, col. 10, lines 35-40). Hooper goes on to teach content is forwarded in a time frame relative to the latency of a semiconductor memory (col. 11, lines 23-32).

It would have been obvious to one of ordinary skill in the art at the time of applicant's invention to modify Rege, Rebec, Cannella, and Singh's invention to include the above mentioned limitation, as taught by Hooper, for the advantage of having a permanent storage medium and to not impede the seamless delivery of video.

Claim 29 contains the limitations of claim 28 and is analyzed as previously discussed with respect to that claim (In reference to fig. 2 in Rege, the second sever module (second server 300) is identical to the first server module (first sever 300). Therefore, the second server module contains the same elements and functions similarly to the first server module).

As for claim 30, Rege teaches wherein the first stream server module further comprises:

a control processor that receives control packets that control how the content is output by the first stream server processor (The packet received by server 300 includes load information - col. 6, lines 30-55).

Claim 33 contains the limitations of claim 28 and is analyzed as previously discussed with respect to that claim.

4. Claims 31 and 32 are rejected under 35 U.S.C. 103(a) as being unpatentable over Rege in view of Rebec (5619528) , Cannella (5854840), Singh (5966722) and Hooper (5414455) as applied to claim 28 above, and further in view of Kondo (7127736).

As for claim 31, Rege in view of Rebec (5619528), Cannella (5854840), Singh (5966722) and Hooper (5414455) disclose the claimed limitations.

In particular, Singh teaches:

an address generator that generates content addresses that are forwarded to the address bus (It is inherent for the system of Singh to generate content addresses which

are forwarded to the address bus such that content can be route to the appropriate location.);

In particular, Rege teaches wherein the first stream server processor further comprises:

a first stream controller comprising:

a payload data buffer that receives content from the data bus – (Since the requested content is buffered in cache 832, the content is sent as buffered data segments to the memory in server 300. Therefore, the memory in server 300 acts as a buffer. – col. 6, lines 30-39);

a control data buffer that receives control data (Control data received includes load information, server, switch and disk failures, rerouting information, priority information, or other positional information necessary. Col. 6, lines 42-46); and

Rebec teaches:

a protocol stream encoder/decoder (841S, 841F, 843S, 843F, 855FA, 855FB, 855SA, 855SB, 851F & 851S) for receiving content –col. 11, lines 30-61.

However, Rege, Rebec, Cannella, Singh, and Hooper fail to teach an encoder/decoder for receiving control data from the control data buffer.

In an analogous art, Kondo teaches a decoder (27-fig. 2) which receives control data (index information) from the control data buffer (35 – fig. 2) – col. 11, lines 1-13, col. 11, line 60 – col. 12, line 15.

It would have been obvious to one of ordinary skill in the art at the time of applicant's invention to modify Rege, Rebec, Cannella, Singh, and Hooper's invention to

include the above mentioned limitation, as taught by Kondo, in order to receive information specifying particular scenes.

As for claim 32, Rege, Rebec, Cannella, Singh, and Hooper and Kondo disclose the claimed limitations. In particular, Rebec teaches wherein the protocol stream encoder/decoder further comprises:

at least two protocol encoder logic modules (855FA & FB, 855 SA & SB) that receives the content and encode the received content into at least two different protocols (col. 11, lines 30-61); and

a protocol select logic module (851F & 851S) that receives the content and forwards it to one of the at least two protocol encoder logic modules (col. 11, lines 30-45).

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the

shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Sumaiya A. Chowdhury whose telephone number is (571) 272-8567. The examiner can normally be reached on Mon-Fri, 9-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, John Miller can be reached on (571) 272-7353. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

SAC

ANDREW Y. KOENIG
PRIMARY PATENT EXAMINER